

FIG 2    A-A

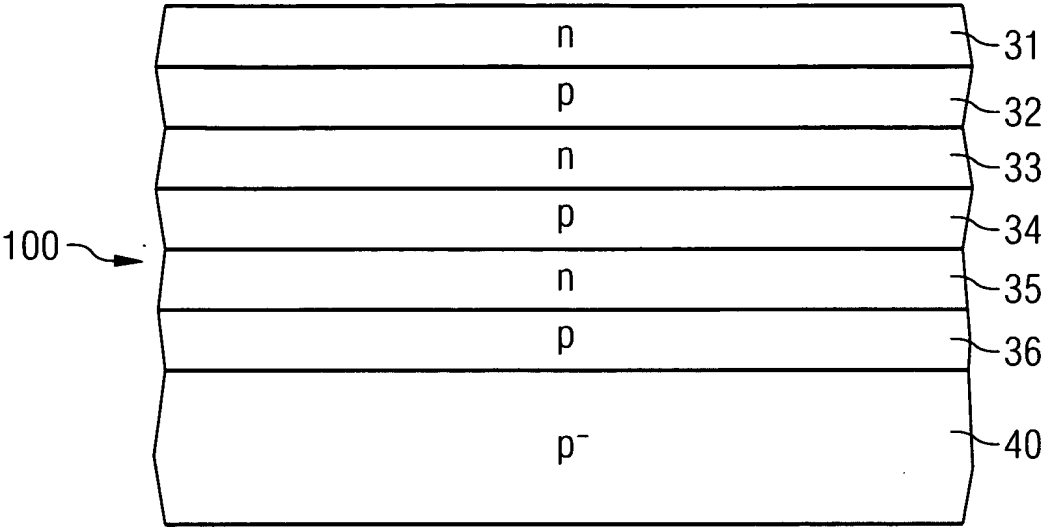


FIG 3

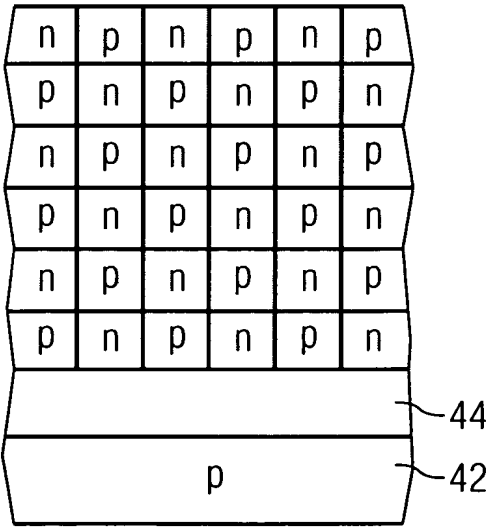


FIG 4 is a cross-sectional view of a semiconductor device. The device includes a substrate 30 composed of several layers labeled 31 through 36. Layer 31 is an n-type layer, while layers 32, 33, 34, 35, and 36 are p-type layers. A gate stack 50 is formed on top of the substrate, consisting of a gate oxide layer 51 and a conductive gate electrode 50. A source/drain region 20 is formed in the substrate, containing an n+ region 21. A channel region 38 is defined by the gate stack 50. Various other regions and interfaces are labeled with numbers 10, 37, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

FIG 5A

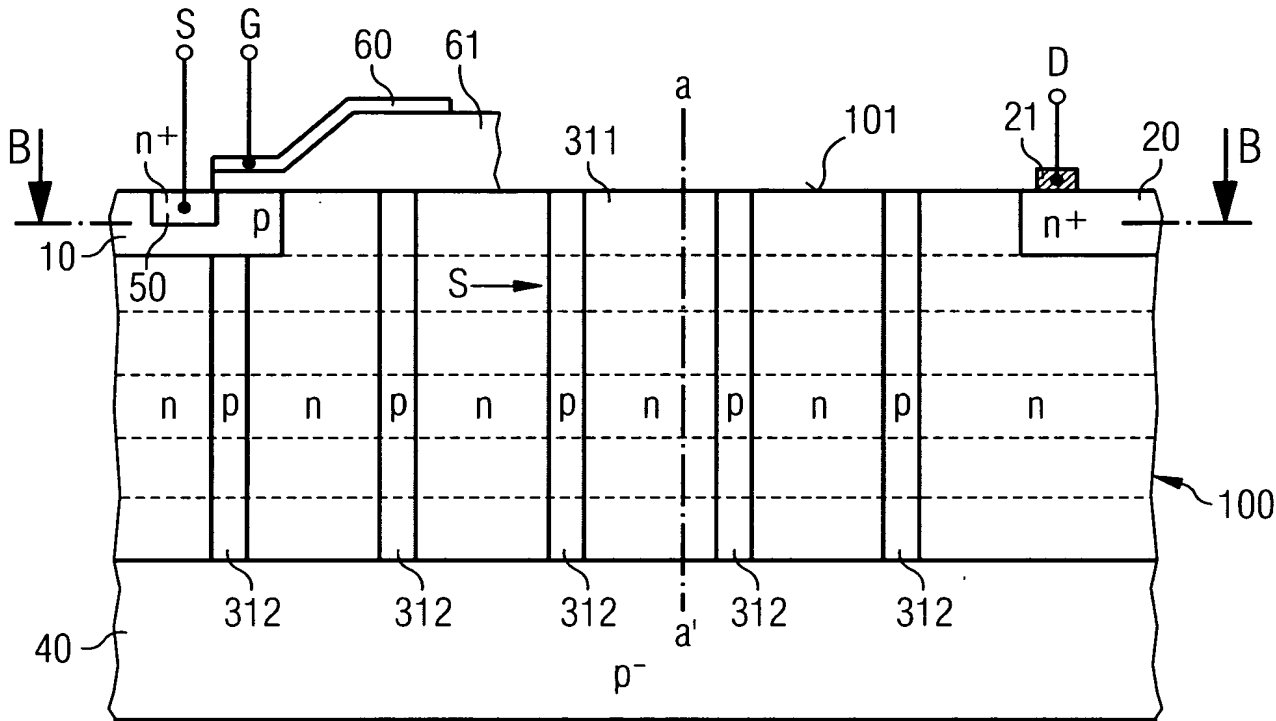


FIG 5B

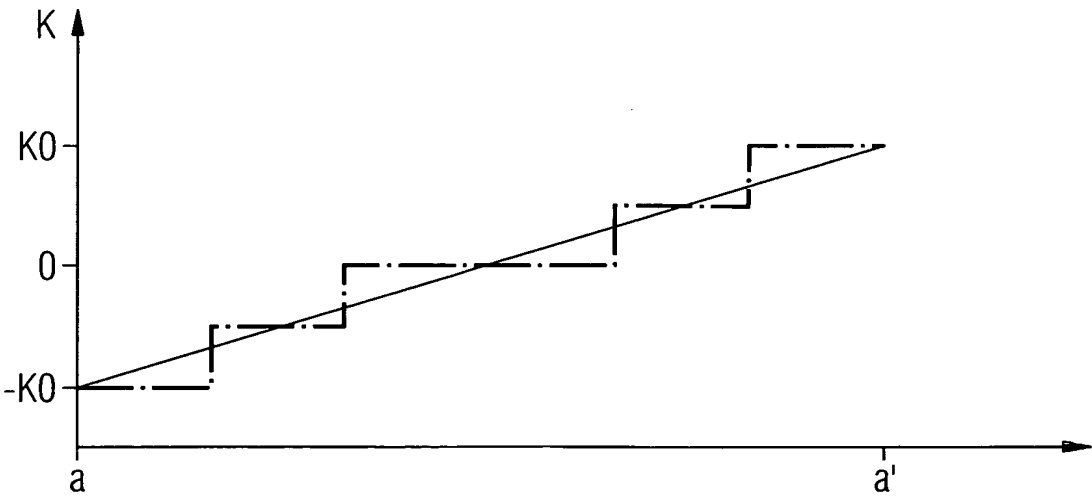


FIG 6 B-B

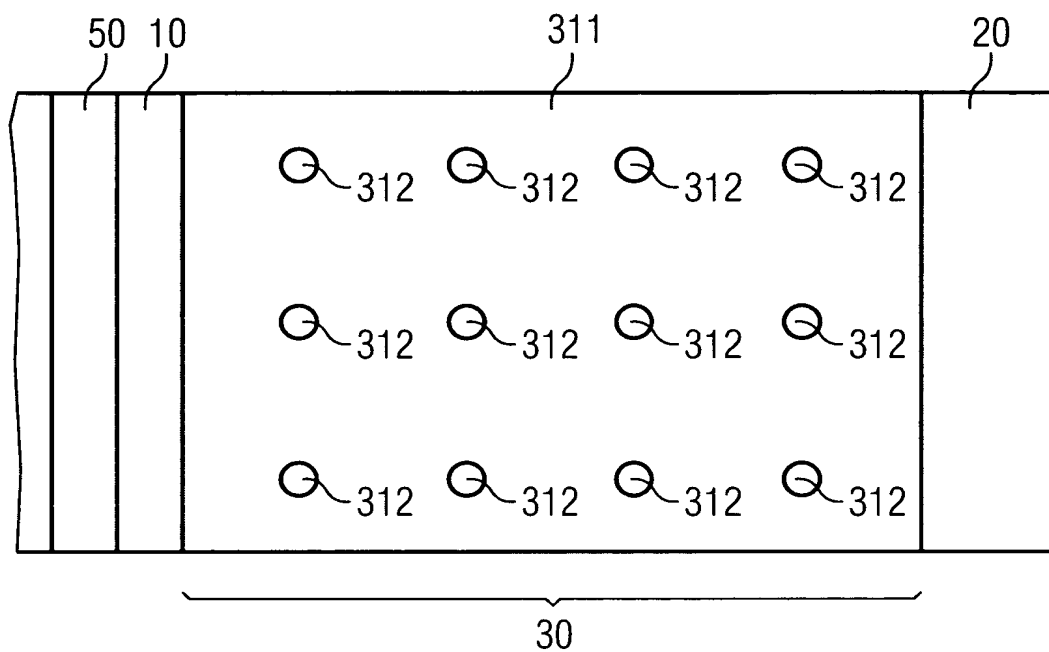


FIG 7

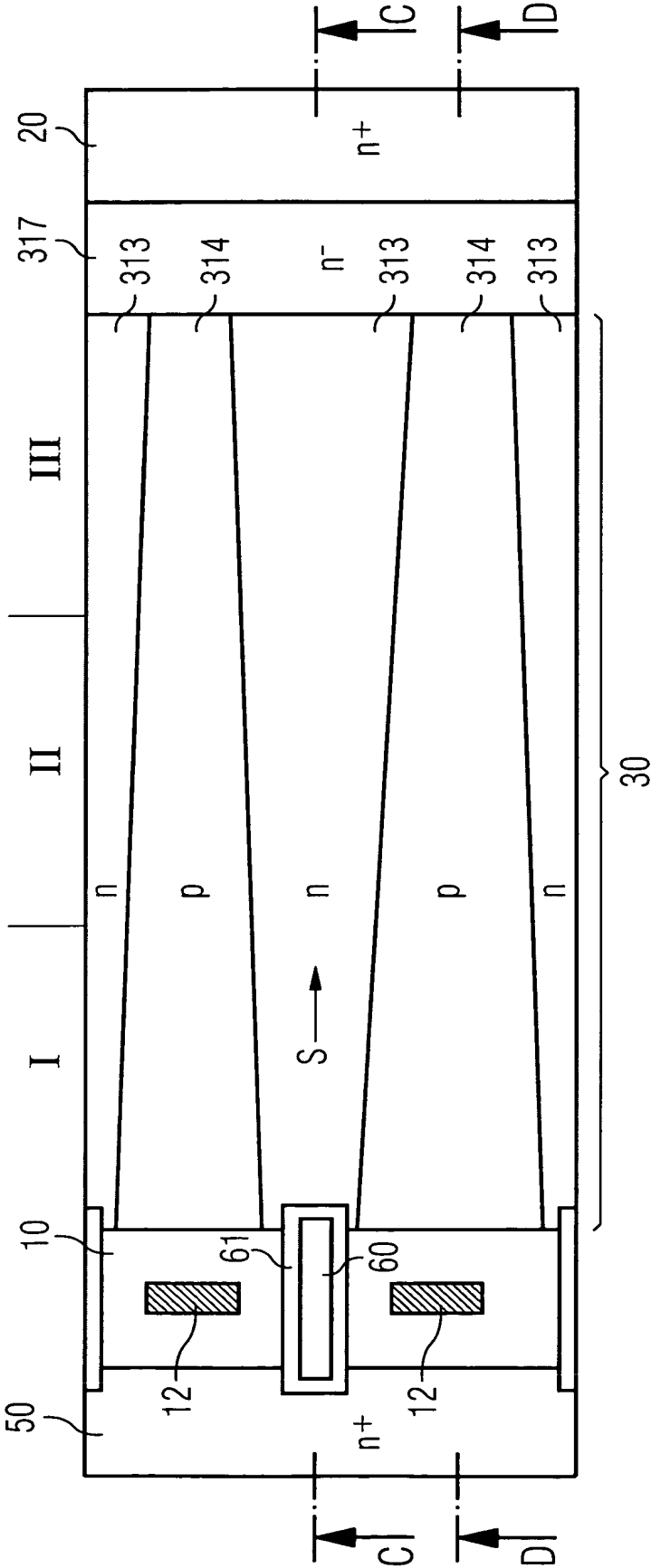




FIG 9

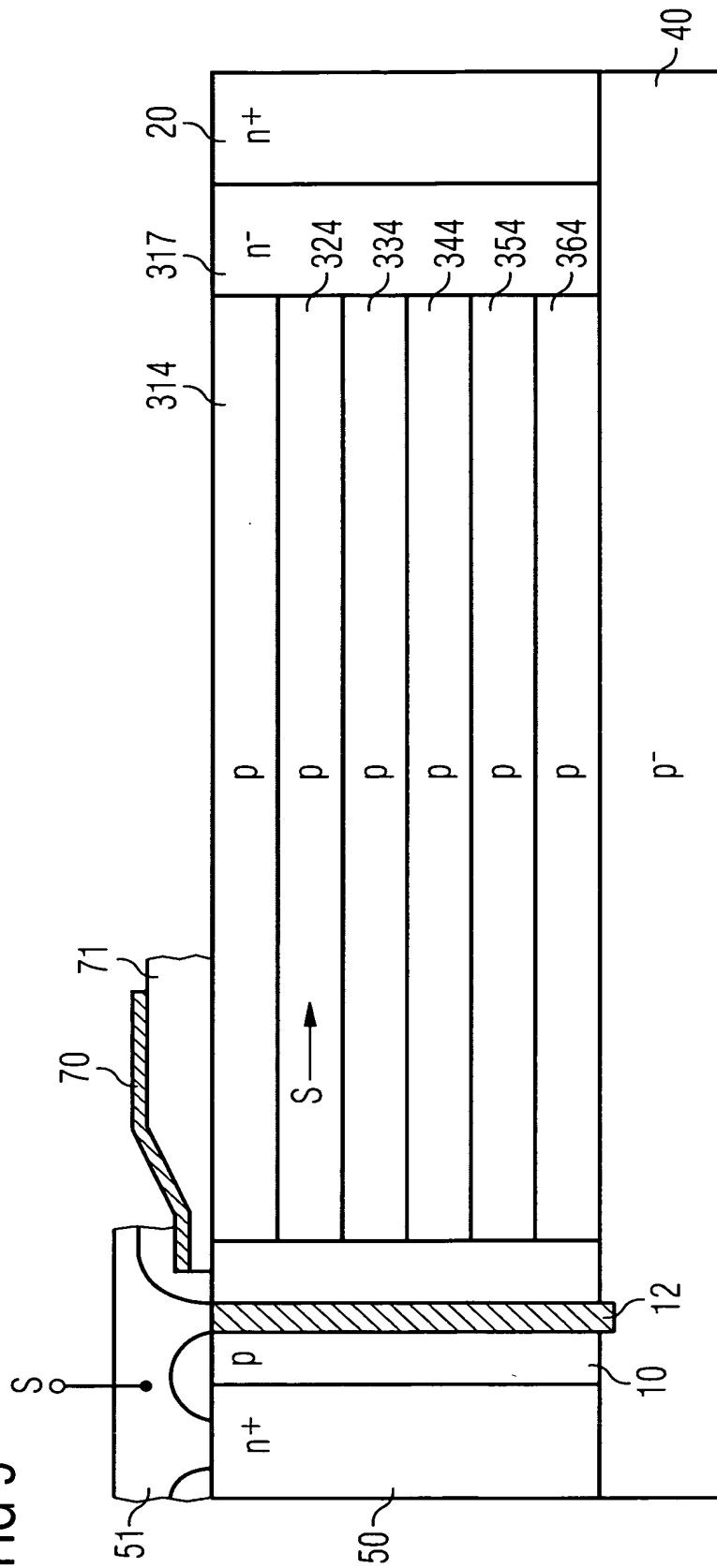




FIG 10

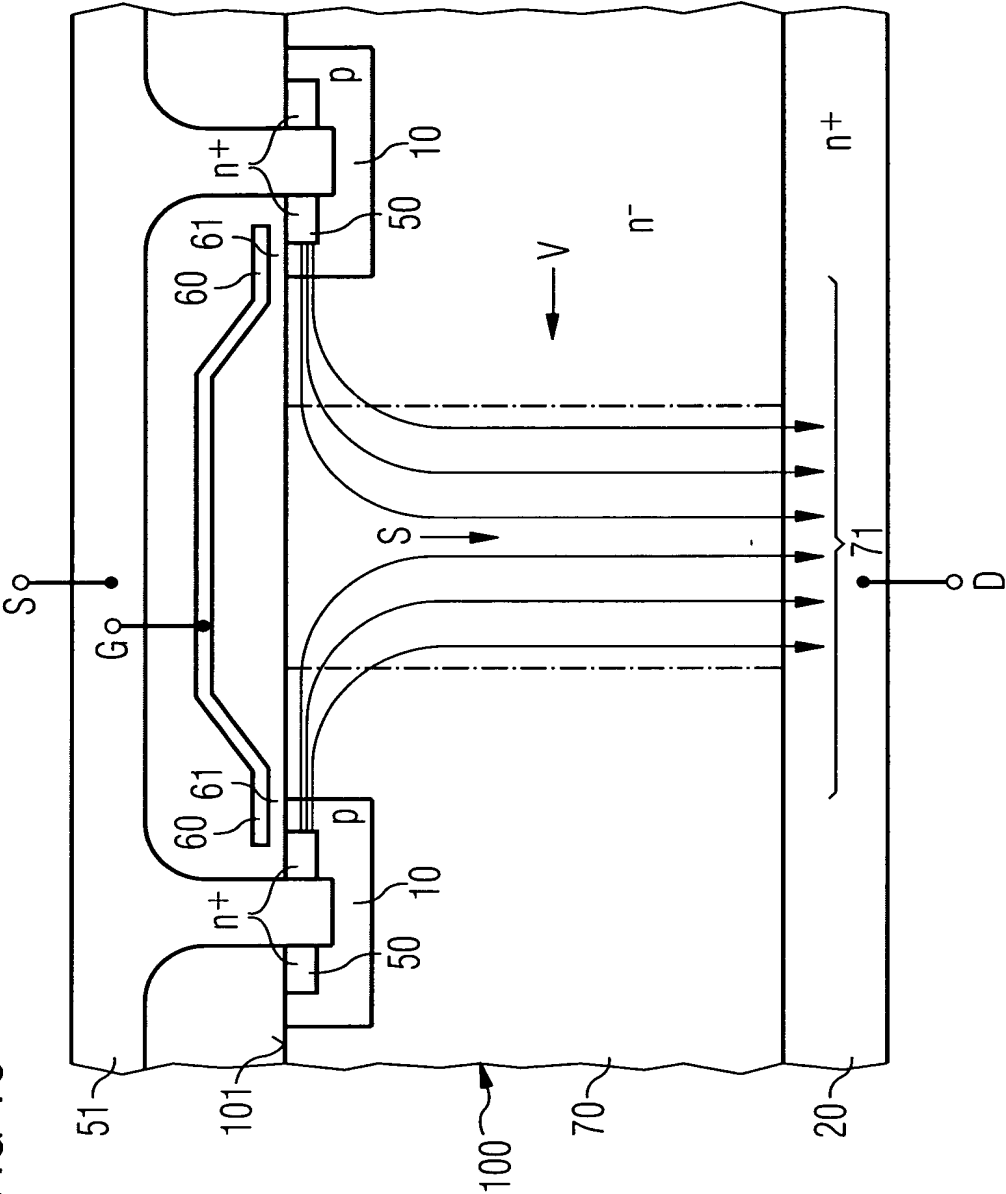


FIG 11

